REMARKS/ARGUMENTS

Claims 1-38 are pending. Claims 4-11, 15-22 and 34-37 are allowed. Claims 1-3, 23 and 30-33 stand rejected. The Examiner also objects to the disclosure, in particular that the text regarding FET 15 improperly refers to the drain and source of the MOSFET 15. As described previously in the response to the last Office Action, the MOSFET is properly described. The source of MOSFET 15 is coupled through resistor RDG to ground. Perhaps the Examiner is confused by the indication of resistor RDG. The nomenclature DG does not refer to drain and ground. RDG was chosen because the resistor can be used for voltage sensing and thus for diagnostic purposes. As described in Fig. 1, the resistor is optional if current is to be monitored with reference to ground. DG is shorthand for "diagnostic".

As previously described, FET 15, which is a P-channel device, is properly identified in the text. Accordingly, it is submitted that the Examiner should withdraw the objection to the disclosure.

With respect to the rejection of claims 1-3, 23 and 30-33, Applicants submit that these claims are allowable over the Osborn et al reference. The Examiner points to the circuit comprising the FET 210, 202 and the sense resistor 222 as the recited current sense circuit. The Examiner points to the drain source voltage as reading on the voltage across FET 210 or the voltage across FET 202 and the recited circuit for producing as the circuitry that generates the potential at node 236 in Fig. 4 of the reference or the circuitry that generates the potential at node 234 which are the inputs to the comparator 230. The Examiner asserts that the comparator recited in the claims is the circuit 230 and that the recited overtemperature protection signal is the output from circuit 230 on line 232.

Applicant respectfully disagrees. Claim 1 recites a power MOS device having a current sense circuit for sensing a current in the power MOS device. For example, this is the power MOS device 10 of Fig. 1 comprising the MOS devices 10A and 10B as well as the circuitry including FETs 15, 17, 30 and 40 whereby the current is reflected as the voltage across the resistor R of Fig. 1, which is provided at the non-inverting input of comparator 50. Claim 1 also recites a circuit for producing a voltage related to the drain source voltage of the power MOS device. This is provided at the inverting input of the comparator 50 which is coupled to the load 20 and the source of the MOSFET 10. The comparator of Fig. 1 is thus coupled to receive at a first input the voltage related to the drain source voltage of the power MOS and at a second input a voltage related to the current in the power MOS device. The comparator generates an

overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs.

In contrast, in the device of the Osborn et al reference, comparator 230 receives at its non-inverting input the voltage across the resistor 238 comprising the output of a current source 240 controlled by a comparator 244. The inputs to the comparator 244 comprise the voltage across the sense resistor 222 as well as the output of a current source 252 measured as a voltage across a resistor 250. Accordingly, the voltage at the non-inverting input of comparator 230 is proportional to the current through the sense resistor 222 which reflects the current in the MOSFET 210.

The inverting input of the comparator 230, that is, node 234, is also coupled to the sense resistor 222. Accordingly, both inputs of comparator 230 are related to the current through the MOSFET 210. In contrast, the comparator according to the present invention is coupled to receive at a first input the voltage related to the drain source voltage of the power MOS device and at a second input the voltage related to the current in the power MOS device. The comparator 230 of the reference is not so configured. It does not receive a voltage related to the drain source voltage of the power MOS device. Accordingly, the Osborn reference fails to teach or suggest the present invention.

Further, according to the present invention, the comparator generates an overtemperature protection signal when the predetermined inequality between the voltages at the first and second inputs to the comparator occurs. In contrast, the comparator 230 according to the Osborn reference merely generates a signal to change the gate drive of the MOSFET transistor 210, 202. It does not produce an overtemperature protection signal.

For the above reasons, it is submitted that claims 1-3, as well as claims 23 and 30-33 are patentable over the Osborn reference and Applicants respectfully request that the Examiner reconsider the rejection of claims and pass this application to issue.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 14, 2004

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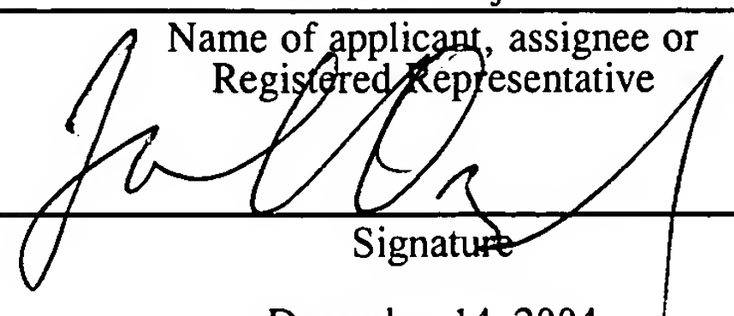
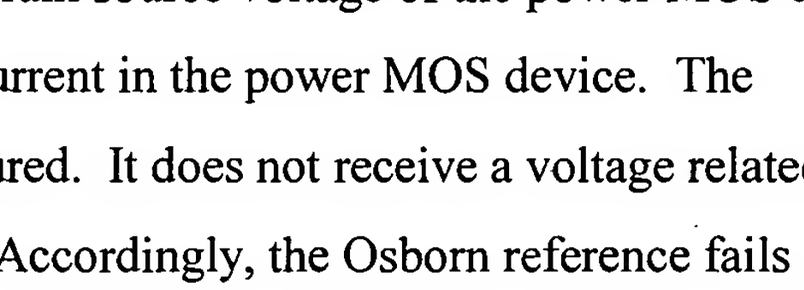


Signature

December 14, 2004

Date of Signature

Respectfully submitted,



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